FIG.1
RELATED ART

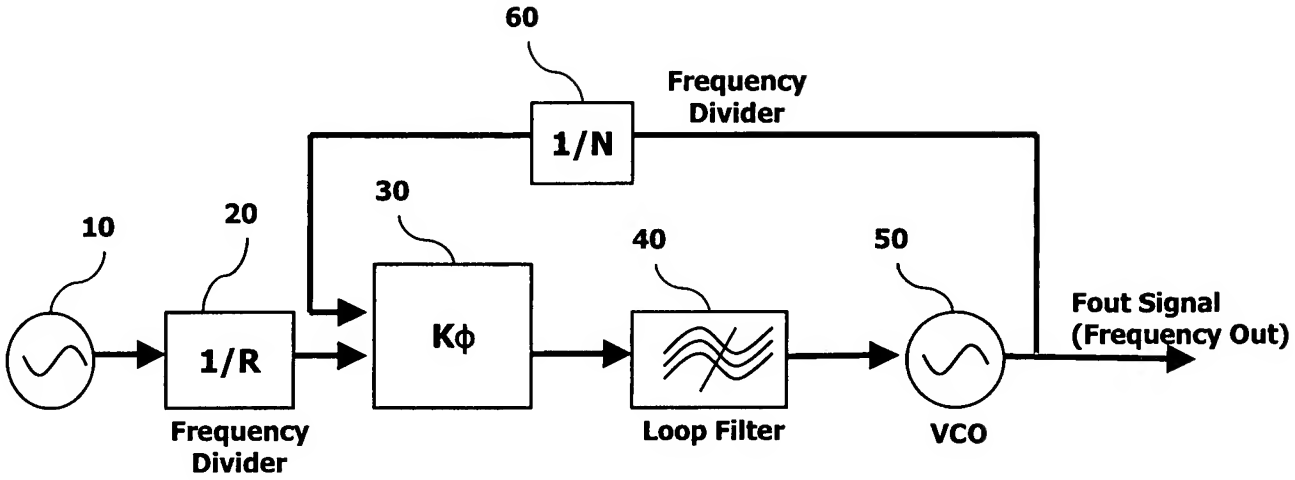


FIG.2
RELATED ART

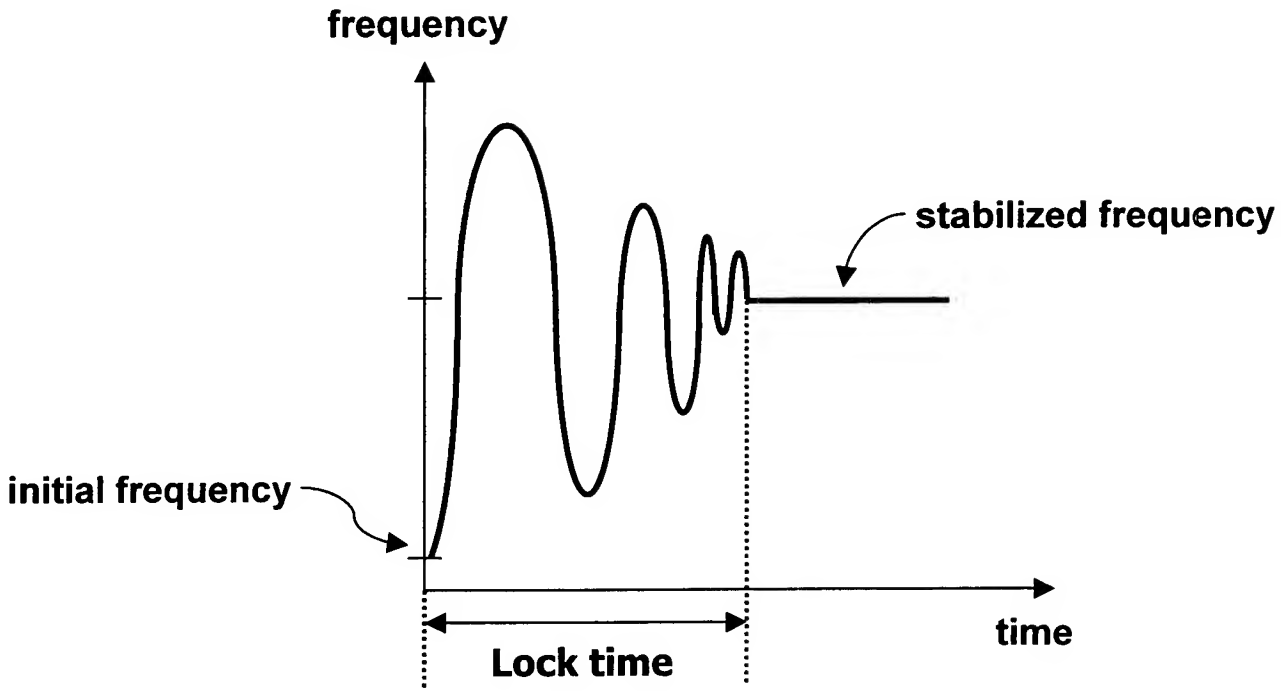


FIG.3

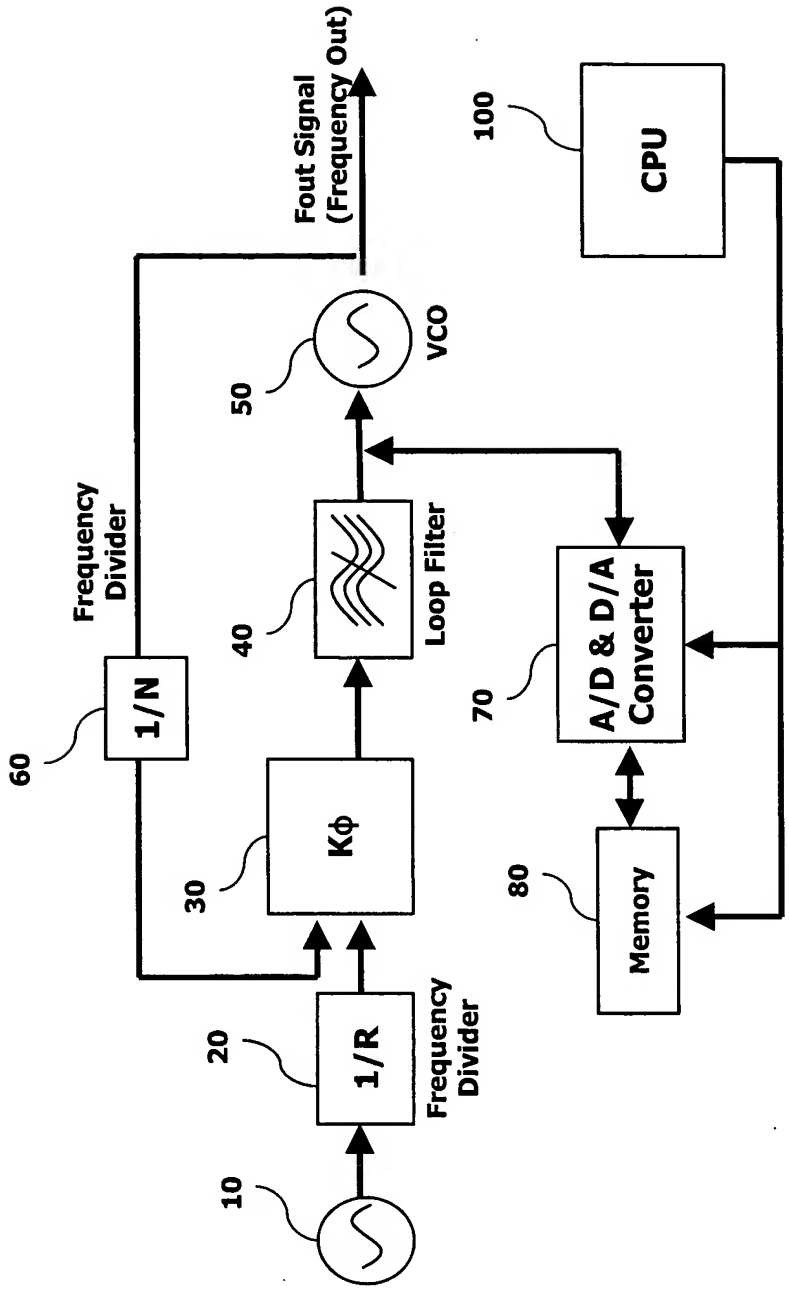

10
20
1/R
Frequency Divider
30
Kϕ
40
Loop Filter
50
VCO
60
1/N
Frequency Divider
Fout Signal (Frequency Out)
70
A/D & D/A Converter
80
Memory
100
CPU

FIG.4

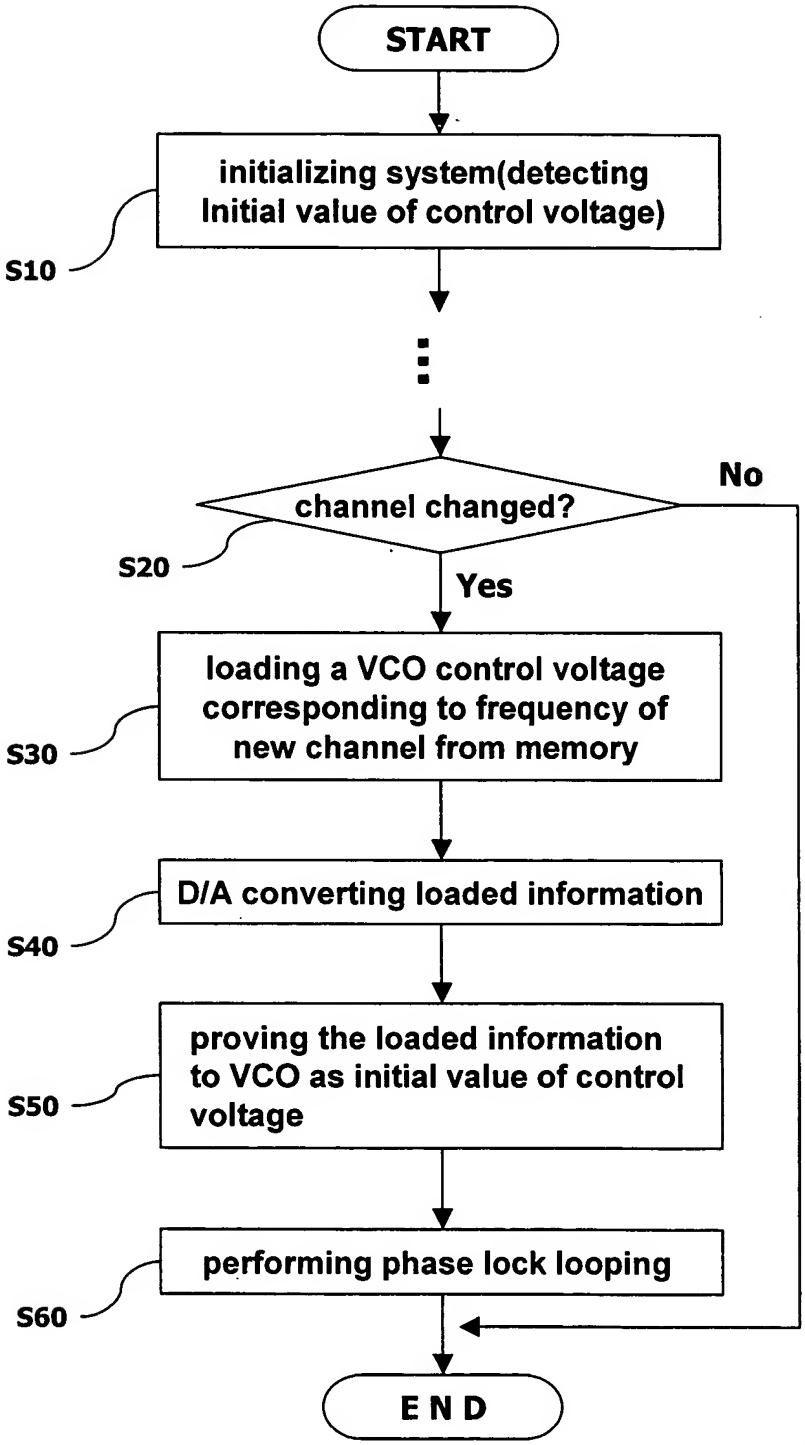
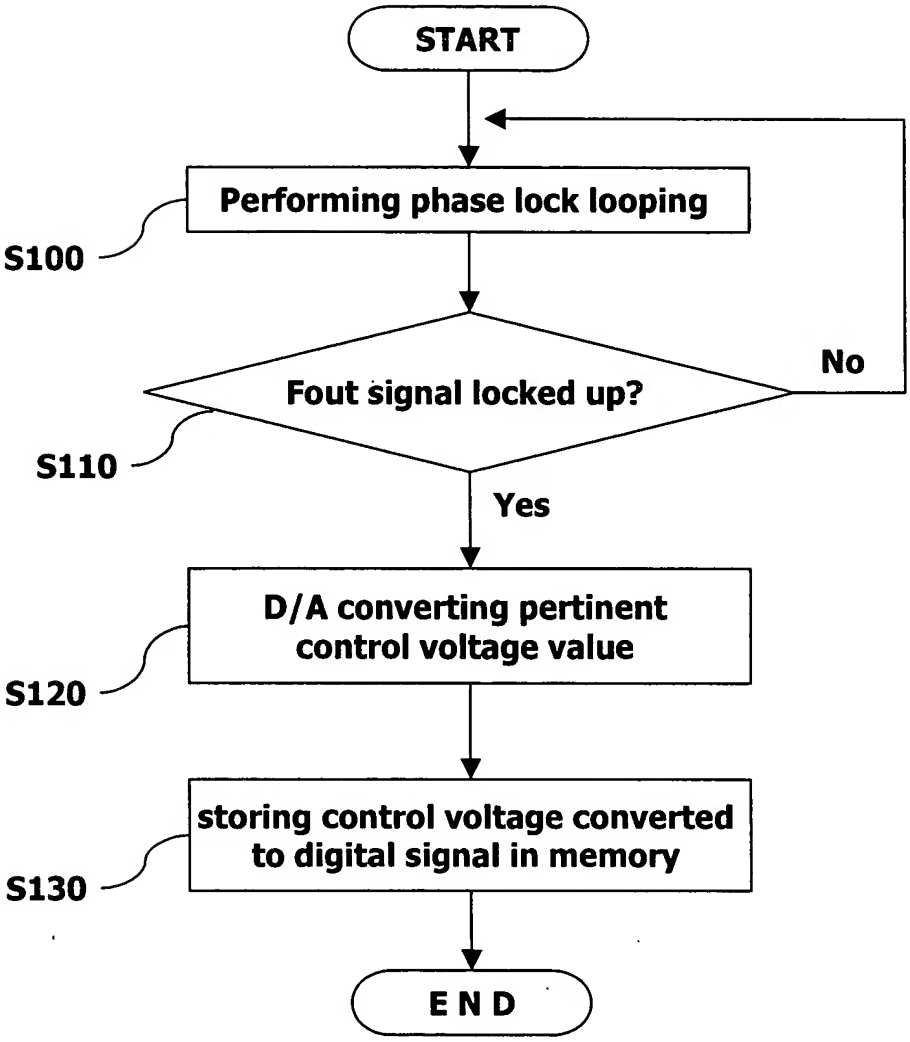

START
initializing system(detecting Initial value of control voltage)
S10
channel changed?
No
S20
Yes
loading a VCO control voltage corresponding to frequency of new channel from memory
S30
D/A converting loaded information
S40
proving the loaded information to VCO as initial value of control voltage
S50
performing phase lock looping
S60
E N D

FIG.5


START
Performing phase lock looping
S100
Fout signal locked up?
No
S110
Yes
D/A converting pertinent control voltage value
S120
storing control voltage converted to digital signal in memory
S130
E N D